25. (new) An integrated circuit comprising:

A. a substrate;

B. operating circuits formed on the substrate, the operating circuits including an operating bus of plural leads for carrying normal operating signals;

C. a serial data input lead formed on the substrate, a serial data output lead formed on the substrate, and a plurality of serial scan paths, each formed of scan registers, formed on the substrate and coupled between the serial data input lead and the serial data output lead, the serial scan paths for carrying serial data signals, including command signals, an expected data pattern signals, and a protocol selection signal, on the substrate,

i. one of the plurality of serial scan paths including a data register having plural data storage locations, a serial input coupled between the serial data input lead and the data storage locations for carrying serial data signals to the data storage locations, a serial output coupled between the serial data output lead and the data storage locations for carrying signals out of the data storage locations, data inputs coupled between the data storage locations and the operating bus for carrying the normal operating signals to the data storage locations, and a control input, and

ii. another of the plurality of serial scan paths including a command register, the command register having plural command storage locations for storing command signals, a control input, a serial input coupled between the serial data input lead and the command storage locations for carrying the command signals to the storage locations, and a serial output coupled to the serial data output lead;

D. an expected data memory formed on the substrate, the expected data memory having plural expected data pattern storage locations for storing an expected data pattern signals and having

at least one input coupled between one of the serial scan paths and the expected data storage locations for receiving the expected data pattern signals from the serial scan path;

E. a comparator formed on the substrate, the comparator having first inputs coupled to the operating bus and second inputs coupled to the expected data memory for comparing at least some of the normal operating signals to corresponding ones of the expected data pattern signals, the comparator having a compare output lead;

F. a mode select input lead formed on the substrate, the mode select input lead for carrying a mode select signal;

G. a serial data clock input lead formed on the substrate, the serial data clock input lead for carrying a serial data clock signal;

H. an access port formed on the substrate, the access port including control circuitry and having a plurality of control outputs, at least one first control output coupled to the control input of the command register, at least one second control output coupled to the control input of the data register, a first input coupled to the mode select input lead and a second input coupled to the serial data clock input lead, the control circuitry being operable selectively to control shifting of the serial data signals between the serial data input lead and the serial data output lead, and into and out of the command register, and into and out of the data register responsive to the mode select signal and the serial data clock signal;

J. a protocol selection memory having at least one storage location for storing a protocol selection signal, and an input coupled to one of the serial scan paths, the protocol selection memory storage location for receiving the protocol selection signal from the serial scan path; and

K. an event control circuit including a protocol input coupled to the protocol selection memory, an event input lead coupled to the compare output lead, and an event output lead.

26. (new) An electrical circuit comprising:

A operating circuits including an operating bus of plural leads for carrying normal operating signals;

B. a serial data input lead and a serial data output lead;

C. an expected data memory having plural expected data storage locations for storing signals representing an expected data pattern;

D. a comparator having first inputs coupled to the operating bus, second inputs coupled to the expected data memory, and a compare output;

E. a command register having plural command storage locations, a control input, a serial input coupled to the serial data input lead and a serial output coupled to the serial data output lead;

F. a data register having plural data storage locations, a control input, data inputs coupled to the operating bus, a serial input coupled to the serial data input lead and a serial output coupled to the serial data output lead;

G. a mode select input lead for carrying a mode select signal;

H. a serial data clock input lead for carrying a serial data clock signal;

I. an access port including control circuitry, the access port having a first input coupled to the mode select input lead, a second input coupled to the serial data clock input lead, at least one first control output coupled to the command register control input, and at least one second control output coupled to the data register control input;

J. a protocol selection memory having at least one storage location coupled to the serial data input lead to store a protocol selection signal; and

K. an event control circuit including a protocol input coupled to the protocol selection memory, an event input lead coupled to the compare output, and an event output lead;

L. the operating circuits, the expected data memory, the comparator, the serial data input lead, the serial data output lead, the command register, the data register, the mode select input lead, the serial data clock input lead, the access port, the protocol selection memory and the event memory being permanently integrated together.

27. (new)An integrated circuit comprising:

A. functional circuits including an operating bus of plural leads;

B. a serial data input lead and a serial data output lead;

C. at least one serial scan path of scan registers coupled between the serial data input lead and the serial data output lead;

D. a protocol selection memory coupled to the at least one serial scan path, the protocol selection memory having at least one storage location to store a protocol selection signal;

E. an expected data memory coupled to the at least one serial scan path, the expected data memory having plural expected data storage locations for storing signals representing an expected data pattern;

F. a comparator having first inputs coupled to the operating bus, second inputs coupled to the expected data memory, and a compare output;

G. an event control circuit including a protocol input connected to the protocol selection memory, an event input lead coupled to the compare output of the comparator, and an event output lead.

28. (new)The integrated circuit of claim 26 including at least one serial scan path of scan registers, the scan registers being coupled between the serial data input lead and the serial data output lead.

29. (new)The integrated circuit of claim 27, or 28 in which the protocol selection memory receives the protocol selection signal from the at least one serial scan path.

30. (new)The integrated circuit of claim 29 in which the expected data memory is coupled to the at least one serial scan path to receive the expected data pattern signals from the serial scan path.

31. (new)The integrated circuit of claim 25, 27, or 28 in which the protocol selection memory is a register in a serial scan path.

32. (new)The integrated circuit of claim 25, 27, or 28 in which there are plural serial scan paths coupled in parallel between the serial data input lead and the serial data output lead, and the protocol selection memory is a register in one of the serial scan paths.

33. (new)The integrated circuit of claim 25, 27, or 28 in which there are plural serial scan paths coupled in parallel between the serial data input lead and the serial data output lead, and the protocol selection memory is coupled to one of the serial scan paths.

34. (new)The integrated circuit of claim 25, 27, or 28 in which the expected data memory is a register in a serial scan path.

35. (new)The integrated circuit of claim 25, 27, or 28 including an enable signal memory coupled to a serial scan path, the event circuits including an enable input lead coupled to the enable signal memory.

36. (new)The integrated circuit of claim 25, 27, or 28 in which the protocol selection memory includes two storage locations, each storing one protocol selection signal, and the event circuit includes two protocol input leads respectively connected to the two storage locations of the protocol selection memory.

37. (new)The integrated circuit of claim 27 in which the event circuit initiates a protocol on the functional circuit, the protocol defined by the protocol selection signal.

38. (new)The integrated circuit of claim 37 further including a data register having plural storage locations, a serial input coupled to the serial data input lead, a serial output coupled to the serial data output lead and data inputs coupled to the operating bus and the plural storage locations, the data register operable to store signals from the operating bus into the storage locations during the selected protocol.

39. (new)The integrated circuit of claim 38 in which the data register is operable to shift the stored signals from the operating bus out of the serial output during the selected protocol.

40. (new)The integrated circuit of claim 35 in which the comparator outputs a match signal on the compare output when at least some of the signals on the first inputs match corresponding signals on the second inputs, the event circuit initiates a

protocol on the functional circuit in response to the match signal and an active enable signal on the enable input lead, the protocol defined by the protocol selection signal.

41. (new)The integrated circuit of claim 26 or 27 in which the comparator outputs a match signal on the compare output when at least some of the signals on the first inputs match corresponding signals on the second inputs, the event circuit initiates a protocol on the functional circuit in response to the match signal, the protocol defined by the protocol selection signal.

42. (new)The integrated circuit of claim 25 or 26 in which the event circuit initiates a protocol defined by the protocol selection signal, the data register is operable to store signals from the operating bus into the plural storage locations and shift the stored data out of the serial output during the protocol.

43. (new)The integrated circuit of claim 42 in which the event circuit initiates the protocol in response to an active event signal on the event input.

44. (new)The integrated circuit of claim 43 in which the active event signal is output from the comparator to the event input when at least some of the first inputs of the comparator match corresponding second inputs to the comparator.

45. (new)The integrated circuit of claim 25, 27, or 28 in which the protocol selection memory includes one storage location storing one protocol selection signal, and the event circuit includes one protocol input lead connected to the one storage location of the protocol selection memory.